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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

FRANKLIN, RICHARD B

ART UNIT	PAPER NUMBER
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2181

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/730,960	Applicant(s) KIM ET AL.	
	Examiner Richard Franklin	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,7,10,20,24,25,27 and 28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,7,10,20,24,25,27 and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1, 3 – 5, 7, 10, 20, 24 – 25, and 27 – 28 are pending.

Response to Arguments

2. Applicant's arguments, see pages 9 – 13, filed 09 April 2007, with respect to the rejection(s) of claim(s) 1 and 20 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of US Patent No. 6,839,774 (hereinafter Ahn).

Drawings

3. The drawings were received on 02 May 2007. These drawings are acceptable.

Claim Objections

4. Claim 3 is objected to because of the following informalities:
 - Claim 3 appends from canceled claim 2, which is improper. The Examiner has believes Applicant intended claim 3 to depend from claim 1, and will treat it as so.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 3, 5, 20, 24, and 27 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,839,774 (hereinafter Ahn) in view of US Patent No. 6,028,445 (hereinafter Lawman).

As per claims 1 and 20, Ahn teaches programming an electronic device (Ahn; Figure 1 Item 100) by transferring program data from outside the electronic device to a buffer circuit (Ahn; Figure 2 Item 134) coupled to a programmable memory (Ahn; Figure 1 Item 130) in the electronic device via a controller circuit (Ahn; Figure 1 Item 160), without using RAM and ROM devices that are separate from the controller circuit (Ahn; Col 5 Lines 39 – 43, Col 7 Lines 8 – 11), that controls programming of the programmable memory (Ahn; Col 2 Lines 60 – 63, Col 5 Lines 39 – 43) in the electronic device that is separate from a general operation processor circuit (Ahn; Figure 1 Item 120) used to provide general operations of the electronic device subsequent to transferring the program data into the programmable memory (Ahn; Col 1 Lines 53 – 59); asserting a signal (Ahn; Figure 1 Item "HALT") to the general operation processor circuit to prevent the general operation processor circuit from accessing the programmable memory during transfer of program data into the programmable memory

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(Ahn; Col 7 Lines 4 – 6, Col 7 Lines 45 – 50); and then de-asserting the signal to the general operation processor circuit to allow the general operation processor circuit to access the programmable memory (Ahn; Col 7 Lines 45 – 50).

Ahn does not teach transmitting an indication to outside the electronic device that the transfer of program data to the programmable memory is complete.

However, Lawman teaches transmitting an indication to outside the electronic device that the transfer of program data to the programmable memory is complete (Lawman; Col 6 Lines 18 – 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ahn to include the indication transmitting because doing so allows for rapid configuration of FPGAs while reducing the cost of any necessary configuration device (Lawman; Col 2 Lines 65 – 67).

As per claim 3, Ahn also teaches wherein the RAM and ROM operate under control of the general operation processor circuit and not under the control of the controller circuit (Ahn; Col 8 Line 56 – Col 9 Line 9).

As per claim 5, Ahn also teaches wherein the transferring the program data further comprises transferring the program data via an Inter-Integrated Circuit interface to the electronic device (Ahn; Col 4 Lines 64 – 66).

As per claim 24, Ahn also teaches wherein transferring the program data further comprises transferring the program data via a Serial Interface to the electronic device (Ahn; Col 4 Lines 61 – 64).

As per claims 27 and 28, Ahn also obviously teaches wherein the buffer circuit comprises a programmable memory word or sector sized buffer circuit because Ahn teaches that data is temporarily stored in the buffer during a long write time (Ahn; Col 6 Lines 19 – 22). From this teaching, it is obvious that the buffer is large enough to store the program data and is therefore at least the size of a word.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,839,774 (hereinafter Ahn) in view of US Patent No. 6,028,445 (hereinafter Lawman) and further in view of US Patent No. 6,295,053 (hereinafter '053 patent).

As per claim 4, Ahn in combination with Lawman teaches the method as described per claim 1 (see rejection of claim 1 above).

Ahn in combination with Lawman does not teach wherein the program data is transferred via a Video Graphics Adapter (VGA) interface.

However, the '053 patent teaches updating program data by sending the program data over a VGA interface ('053; Figure 3 Item 18, Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ahn in combination with Lawman to include the VGA interface because doing so allows for programming of the

device without the need for a special programming port or interface ('053; Col 6 Lines 61 – 67).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,839,774 (hereinafter Ahn) in view of US Patent No. 6,028,445 (hereinafter Lawman) and further in view of US Patent No. 5,968,141 (hereinafter Tsai).

As per claim 7, Ahn in combination with Lawman teaches the method as described per claim 1 (see rejection of claim 1 above).

Ahn in combination with Lawman does not explicitly teach wherein the general operation processor circuit accessed separate RAM and ROM to provide general operations of the electronic device.

However, Tsai teaches wherein the general operation processor circuit accesses separate RAM (Figure 3 Item 35) and ROM (Figure 3 Item 34) to provide general operations of the electronic device (Tsai; Col 4 Lines 63 – 67, Col 6 Lines 34 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ahn in combination with Lawman to include the separate RAM and ROM accessing because doing so allows for the general operation processor to have a working memory space (Tsai; Col 4 Lines 63 – 67).

8. Claims 5 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,839,774 (hereinafter Ahn) in view of US Patent No. 6,028,445

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(hereinafter Lawman) and further in view of US Patent No. 6,507,881 (hereinafter Chen).

As per claims 5 and 25, Ahn in combination with Lawman teaches the method as described per claim 1 (see rejection of claim 1 above).

Ahn in combination with Lawman does not teach cycling power provided to the controller circuit to reset the controller circuit.

However, Chen teaches re-booting the system when the programming has completed (Chen; Col 4 Lines 14 – 16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ahn in combination with Lawman to include the power cycling because doing so would allow for the system to return to a normal operating mode (Chen; Col 4 Lines 14 – 16).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
Patent Examiner
Art Unit 2181



ALFORD KINDRED
PRIMARY EXAMINER